<u>AMENDMENTS TO THE SPECIFICATION</u>

<u>IN THE ABSTRACT</u>:

Please replace the original Abstract with the amended Abstract on the accompanying separate sheet.

<u>IN THE SPECIFICATION</u>:

Please replace the following paragraphs at page 9, lines 6-9, with the following amended paragraphs.

~~Fig. 6 is a~~ <u>Figs. 6A-6C are</u> sectional ~~view~~ <u>views</u> illustrating the process for producing the semiconductor memory device in Example 1;

~~Fig. 7 is a~~ <u>Figs. 7A-7C are</u> sectional ~~view~~ <u>views</u> illustrating the process for producing the semiconductor memory device in Example 1;

Please replace the paragraph beginning at page 12, line 25, with the following amended paragraph.

Fig. 2 is a plan view, in which metal wiring is omitted unless necessary for illustration. The part (21) surrounded by a dotted line represents a unit cell. The cross section taken along the line A-~~A~~<u>B</u> corresponds to Fig. 1. The

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structure having 64 word lines arranged in the Y-direction of the diagram constitutes a basic unit (which is referred to as a memory mat hereinafter). At its end, the assist electrodes (4, 8, 9) are bundled alternately (24, 30), so that a voltage can be applied independently to the adjacent assist electrodes. At this end, there is a trench filled with an insulating film for element isolation, so that active regions are separated from each other. The diffusion layers (2, 3) are connected to these active regions (32, 27). There are gate electrodes (28, 25) between these diffusion layers (2, 3) and the contacts (26, 41) to wiring. They constitute the MOS transistor for selection. This selective MOS makes a connection between the local bit lines (2, 3, 6, 7) of diffusion layer and the global data lines (34, 35, 33, 36). To one global data line are connected a plurality of local data lines, and this constitutes the hierarchical data line structure. This structure produces an effect of reducing the capacity to be charged and discharged, increasing the operating speed, and decreasing power consumption. In addition, this structure obviates the necessity of applying a high data line voltage to the memory cell except when writing is performed in a selected memory mat. This leads to a reduction of disturbance passing to unselected cells. Another advantage is that the source line

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of inversion layer (which has a comparatively high resistance) can be made short in the reading operation (which will be mentioned later). This is effective in increasing the reading speed. Another feature is that there exists a structure in which the assist electrode (4) overlaps with the active region (22) containing an n-type impurity introduced thereinto. The assist electrode (4) and the active region (22) are insulated from each other by the insulating film formed on the surface of the substrate. This active region is connected to the metal wiring (23) through the contact structure. The advantage of this structure is that a potential can be applied to the inversion layer (1) from the metal wiring (23) through the active region (22) when a positive voltage is applied to the assist electrode (4) and the inversion layer (1) is formed in the surface of the substrate under the gate. The assist electrodes on both sides also have a region which overlaps with the region containing an n-type impurity introduced thereinto and the contact structure and wiring (29) to apply a potential to this region.

Please replace the paragraphs at page 24, line 22 through page 28, line 10, with the following amended paragraphs.

The production process in this Example will be explained with reference to Figs. 6A to 9. Figs. 6A-6C are ~~Fig. 6 is a~~ sectional ~~view~~ views of the memory cell. Figs. 7A-7C and 8 are sectional views showing the p-type and n-type transistors in the peripheral circuit. A p-type silicon substrate (16) is used. After an element isolating region (39) has been formed, a deep n-type well (15) is formed and a p-type well (14) is further formed. As is apparent from Fig. 2, there is no element isolating region in the array of memory cells because element isolation in that part is accomplished electrically by the assist electrodes. It exists only at the lead to the contact of each region at the mat end and at the part of peripheral circuit. Ion implantation is performed to adjust the threshold voltage of the peripheral circuit with high voltage resistance, and ion implantation with B (boron) for adjustment of threshold voltage is performed on the region where memory cells are formed. A gate insulating film (20 nm thick) is formed for the transistor with high voltage resistance, and the gate insulating film on the surface of the substrate in the region of memory cells and the region of peripheral circuits with ordinary voltage resistance is removed by using the resist as a mask. The surface of the

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substrate is oxidized again, so that an SiO_2 film (18), which is 6 nm thick, is formed. A non-doped polysilicon film (38) is formed by CVD (Chemical Vapor Deposition), which is to be made later into the assist electrodes (4, 8, 9) and the gate electrodes of the peripheral circuits. P ion implantation and BF_2 ion implantation are performed by using the resist as a mask to form the n-type gate region and the p-type gate region, respectively. Further, a CVD-SiO_2 film is deposited on the polysilicon film, and the pattern for the assist electrodes (4, 8, 9) is formed by using the resist as a mask. See Fig. ~~6(a)~~6A. However, at this time, the pattern of the gate electrode for the peripheral circuits is not formed, and it is left covered with the polysilicon film and CVD-SiO_2 film. See Fig. ~~7(a)~~7A. After that, CDV-SiO_2 is deposited up to 10 nm, and ion implantation is performed for adjustment of the impurity concentration in the surface of the substrate under the charge storage regions (10, 11) by using this film as the implant through film.

Subsequently, CDV-SiO_2 is deposited up to 10 nm and further polysilicon is deposited up to 100 nm. Etch-back is performed to form the polysilicon side wall (43) on the side of the assist electrode. Using this side wall as a mask, As (arsenic) ion implantation is performed to form the n-type

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diffusion layer regions (2, 3, 7). See Fig. ~~6 (b)~~ 6B. Dry etching is performed to remove the polysilicon side wall, and then wet etching with HF is performed to expose the surface of the substrate. Subsequently, oxidation up to 8 nm is performed ~~to form~~ and silicon fine crystal grains are deposited. In the trial product, they have an average particle diameter of 16 nm and a density of $3 \times 10^{11}/cm^{-2}$. Then, plasma oxidation is performed to oxidize (up to 4.5 nm) the surface of the silicon fine crystal particles. Silicon fine crystal particles are deposited again. In this way it is possible to form fine crystal grains in high density without contact with one another, and they store more electrons under the same writing conditions. This leads to stable characteristics with a broader margin between one stored information and another. In this example, deposition is performed twice, however, it is permissible to repeat plasma oxidation and fine crystal grain deposition as many times as required. Unlike thermal oxidation, plasma oxidation does not promote oxidation more than radical intrusion. Therefore, it has no possibility that the initially formed crystal grains are made very small and the tunnel insulating film is made thick by repeated plasma oxidation. After that, CVD-SiO_2 (as the interlayer insulating film) is deposited up to 12 nm. A polysilicon

film (doped in n-type) and a W (tungsten) film are deposited to form a double-layer structure. Using the resist as a mask, etching is performed to form the word line (5). See Figs. ~~6(e)~~6C and ~~7(b)~~7B. Using the resist as a mask, etching is performed on the polysilicon film (38) in the region of peripheral circuits, the dots (17) on the laminate structure of $CVD-SiO_2$, and the interlayer insulating film (20) thereon. After that, using the resist as a mask, the gate electrodes (41, 42) of the transistors of the peripheral circuit are formed. See Fig. ~~7(e)~~7C. Using this gate pattern and the resist as a mask, ion implantation is performed to form a shallow p-type region (47) in p-MOS and a shallow n-type region (46) in n-MOS. $CVD-SiO_2$ is further deposited, and etch back is performed to form the side wall (40). Using this side wall (40) and the resist as a mask, ion implantation is performed to form a p-type diffusion region (45) in p-MOS and an n-type diffusion region in n-MOS (44). See Fig. 8. An interlayer film is deposited and planarization is performed, and the contact process and wiring process are performed.

Please replace the paragraph at page 31, line 11 through page 34, line 15, with the following amended paragraph.

The writing operation is explained first. A positive voltage is applied to the assist electrodes (48, 49) at both sides of the cell (60) in which writing is to be made, so that the inversion layers (50, 51) are formed in the surface of the substrate under them. The adjacent assist electrodes are set at a low voltage (say, 0 V) which is low enough not to form the inversion layer, so that elements are electrically isolated. When the inversion layer is formed, the n-type diffusion layer regions (61, 62) conduct to the inversion layer, so that it is possible to apply a voltage to the global data lines (34, 35) through the contacts (57, 58) formed in the diffusion layer region. Between the adjacent assist electrodes, 4-bit information is stored at two places (10, 11). For the writing of information in the memory node near the assist electrode (48) at one end, this electrode (48) is set at a voltage (say, 2 V) which is high enough to form the high-resistance inversion layer. The data line (34) to supply voltage to the inversion layer (50) under this electrode is set at 0 V. The data line (35) to supply voltage to the inversion layer under the assist electrode (49) at the other end is set at 4 V. The corresponding assist electrode (49) is set at a voltage (say, 7 V), which is sufficiently higher than the set

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voltage (4 V in this case), so that a low-resistance inversion layer is formed. When a high voltage pulse (say, 15 V~~, 3 μs~~) is applied to the control electrode (5) under this state, the electric field concentrates at the boundary between the inversion layer (50) under the assist electrode (48) at one end and the inversion layer under the control electrode ~~(50)~~ (5), thereby giving rise to hot electrons. The thus generated hot electrons are attracted by the control electrode (5) toward the electric field in the direction perpendicular to the control electrode (5), and they burst into the neighboring memory node (10). In this situation, the inversion layer (50) under the assist electrode (48) at one end has a high resistance and hence the current flowing along the wiring (50, 51) of the inversion layer is not so large. Thus, the amount of electrons to be injected into the memory node can be made large relative to the current that flows. This means that there is no possibility of current becoming excessively large at the time of writing in a large number of cells. This is desirable for files to and from which a large number of bits are input and output at one time. Example 2 is identical to Example 1 in that more than one pulse of the control electrode is used according to the threshold value level to be written and writing is performed while

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verification is being performed. In the case where it is driven by the selective word line and the selective assist electrode pair and injection of electrons is not desirable because writing has been completed or the cell is not the one in which the threshold value level is not to be written, the voltage to be supplied to the diffusion layer (51) is made equal to that of the diffusion layer (5) at the other end, so that the occurrence of hot electrons is prevented. In the case where it is desirable to write information in the other end (11) of the cell, the object is achieved by replacing the settings of the assist electrodes (48, 49), the data lines (34, 35), and the inversion layer wirings (50, 51). In the case of this constitution, the assist electrodes (8, 9) at both sides of the assist electrode pair (48, 49) constituting the relevant cell is used for element isolation at the time of writing and reading; therefore, it is possible to make active its adjacent assist electrode (63). In other words, it is possible to operate the three assist electrodes as one set; however, it is convenient to operate the four assist electrodes as one set from the stand point of use and control. In this case, therefore, control is performed on the four assist electrodes as one set. Consequently, unlike Example 1, the assist electrodes (48, 49, 8, 9, 63, 64) are made into bundles (53, 54, 55, 56) for

every four units.   As in Example 1, this example also employs the hierarchical data line structure.   Therefore, it produces the same effect as in Example 1, and it also produces a new effect at the time of writing operation.   The hierarchical design permits the inversion layer formed under the assist electrode to be short.   This reduces the variation of voltage effect that depends on the position. Moreover, the voltage effect itself is small and hence it is only necessary to apply a small voltage to the inversion layer at the time of writing.

Please replace the paragraph at page 54, line 12 through page 55, line 7, with the following amended paragraph.

In the above-mentioned writing system, the writing terminates automatically when the charge stored in the inversion layer has been discharged completely.   The amount of charge (Qg) injected into the charge storage region (11) is represented by Qg = Qi × γ (where γ denotes the injection efficiency).   Here, the injection efficiency γ is a function of the potential of the charge storage region (11), the drain voltage, and the voltage of the assist electrode (67).   It is assumed to be constant although it

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varies during the writing operation. The dependence of the injection efficiency $\beta\gamma$ on the voltage of the assist electrode is comparatively small. For example, when the voltage of the assist electrode fluctuates between ± 0.1 V, the value of $\beta\gamma$ varies by only 0.3 order of magnitude. Since the charge Qd stored in the inversion layer is constant, the Qg (which represents the writing characteristics) varies by only 0.3 order of magnitude. The writing method in Example 3 suffers variation by one order of magnitude or more, whereas the writing method in this example is very little subject to variation. This leads to a reduction in time for writing.

Please replace the paragraph at page 59, line 19 through page 60, line 14, with the following amended paragraph.

In the above-mentioned writing system, the writing terminates automatically when the charge stored in the inversion layer has been discharged completely. The amount of charge (Qg) injected into the charge storage region (10) is represented by Qg = Qi $\times$ $\beta\gamma$ (where $\beta\gamma$ denotes the injection efficiency). Here, the injection efficiency $\beta\gamma$ is a function of the potential of the charge storage region

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(10), the drain voltage, and the voltage of the assist electrode (48). It is assumed to be constant although it varies during the writing operation. The dependence of the injection efficiency $\beta\gamma$ on the voltage of the assist electrode is comparatively small. For example, when the voltage of the assist electrode fluctuates between ±0.1 V, the value of $\beta\gamma$ varies by only 0.3 order of magnitude. Since the charge Q_d stored in the inversion layer is constant, the Q_g (which represents the writing characteristics) varies by only 0.3 order of magnitude. The writing method in Example 1 suffers variation by one order of magnitude or more, whereas the writing method in this example is very little subject to variation. This leads to a reduction in time for writing.